

03560.002863



*Cole #*  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: )  
KIMIHIKO FUKAWA ) : Examiner: Houshang Safaipour  
Appln. No.: 09/902,703 ) : Art Unit: 2627  
Filed: July 12, 2001 ) :  
For: IMAGE PROCESSING APPARATUS ) :  
U.S. Patent No.: 7,002,713 B2 ) :  
Issued: February 21, 2006 ) July 17, 2006

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**  
JUL 21 2006  
**of Correction**

**CERTIFICATE OF CORRECTION**  
UNDER RULES 322 AND 323

Sir:

It is respectfully requested that a Certificate of Correction be issued by the Patent and Trademark Office due to errors which appear in the printed patent as a result of Patent and Trademark Office mistakes, and mistakes of a clerical, typographical, or minor character, which were not the fault of the Patent and Trademark Office. A Certificate of Correction form, in duplicate, is enclosed.

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JUL 24 2006

Patentee's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "John A. Krause", written over a horizontal line.

John A. Krause  
Attorney for Patentee  
Registration No. 24,613

FITZPATRICK, CELLA, HARPER & SCINTO  
30 Rockefeller Plaza  
New York, New York 10112-3801  
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UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,002,713 B2

DATED : February 21, 2006

INVENTOR(S) : KIMIHIKO FUKAWA

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 5

Line 54, "row." should read

--row;

a first output line, connected to each first pixel row of each of said plurality of sensor chips to receive first pixel signals from each first pixel row of each of said plurality of sensor chips; and

a second output line, connected to each second pixel row of each of said plurality of sensor chips to receive second pixel signals from each second pixel row of each of said plurality of sensor chips.--;

Line 62, "row ," should read --row,--;

Line 67, "row." should read

--row;

a first output line provided outside said plurality of sensor chips, to which a signal from said first pixel row in each of said plurality of sensor chips is read; and

a second output line provided outside said plurality of sensor chips, to which a signal from said second pixel row in each of said plurality of sensor chips is read;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to said first output line and said second output line; and

a combining circuit provided outside said plurality of sensor chips and connected to said first and second output lines to receive signals from said first and second output lines from the first and second pixel rows of each of said plurality of sensor chips, which selectively outputs the signals from said first output line and said second output line, wherein said combining circuit is common to said plurality of sensor chips.--.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

COLUMN 6

Line 40, "chip" should read --chips--; and  
Line 60, "conflaured" should read --configured--.

COLUMN 7

Line 11, "signals" should read --signal--.

COLUMN 8

Line 1, "imagine" should read --imaging--.

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Line 54, "row." should read

--row;

a first output line, connected to each first pixel row of each of said plurality of sensor chips to receive first pixel signals from each first pixel row of each of said plurality of sensor chips; and

a second output line, connected to each second pixel row of each of said plurality of sensor chips to receive second pixel signals from each second pixel row of each of said plurality of sensor chips.--;

Line 62, "row ," should read --row,--;

Line 67, "row." should read

--row;

a first output line provided outside said plurality of sensor chips, to which a signal from said first pixel row in each of said plurality of sensor chips is read; and

a second output line provided outside said plurality of sensor chips, to which a signal from said second pixel row in each of said plurality of sensor chips is read;

a driving circuit, which drives said plurality of sensor chips to sequentially output signals to said first output line and said second output line; and

a combining circuit provided outside said plurality of sensor chips and connected to said first and second output lines to receive signals from said first and second output lines from the first and second pixel rows of each of said plurality of sensor chips, which selectively outputs the signals from said first output line and said second output line, wherein said combining circuit is common to said plurality of sensor chips.--.

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